#6/1-9-03
V. Jones

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Mirmajid Seyyedy et al.	Examiner: Guy J Lamarre
Serial No.:	09/239,898	Group Art Unit: 2133
Filed:	January 29, 1999	Docket: 303.550US1
Title:	METHOD AND APPARATUS FOR TESTING A MEMORY DEVICE WITH COMPRESSED DATA USING A SINGLE OUTPUT	

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RESPONSE UNDER 37 CFR § 1.111

Commissioner for Patents
Washington, D.C. 20231

In response to the Office Action dated 3 October 2002, the applicant respectfully requests reconsideration of the above-identified application in view of the following remarks. Claims 1-41 and 43-45 are pending in the application, and are rejected. None of the claims has been amended.

Rejection of Claims under §102

Claims 1, 2, 4-6, 8-10, 12-28, 30-41, and 43-45 were rejected under 35 USC § 102(e) as being unpatentable over Matsumura et al. (U.S. Patent No. 5,991,232, Matsumura). The applicant respectfully traverses.

Matsumura issued on 23 November 1999, which is after the 29 January 1999 filing date of the above-identified application. The applicant does not admit that Matsumura is prior art, and reserves the right to swear behind Matsumura at a later date.

Claim 1 recites a circuit comprising, among other elements, a compression circuit structured to generate compressed data based on data values and an output circuit coupled to the compression circuit and being structured to produce the compressed data at a single output on edges of a clock signal.

Matsumura shows a clock synchronous memory and in Figures 21-22 a compression circuit 4j. The compression circuit 4j is described in Matsumura from column 21, line 16 to column 22, line 25. The compression circuit 4j of Matsumura compresses 256 bits down into a single bit ECMP with EXOR circuits 4j0-4j7 and an AND circuit 4ja. The single bit ECMP is then transferred through a latch 4k to a pad 8p.